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INSTALLATION GUIDE

NS23M

256K BYTE MEMORY

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National Semiconductor Corporation												
2900 Semiconductor Drive, Santa Clara, Calif. 95051												

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CHAPTER I INSTALLATION AND MAINTENANCE

1.1 INTRODUCTION

This section will provide the information necessary to install the NS23M, install or remove any of the options, and maintain the memory. Table 1.1 lists the configuration jumpers and a description of each, Table 1.2 lists the switches and their functions and Figure 1.1 shows the placement of the jumpers and switches.

W1*	I. = 200 ns DRAM R. = 150 ns DRAM
W2*	I. = 150 ns DRAM R = 200 ns DRAM
W3*	I. = Test Only R = Standard Configuration
W4*	I. = Standard Configuration R = Test Only
W5*	I = 32K DRAM R = 16K or 64K DRAM
W6*	I = 64K DRAM R = 16K or 32K DRAM
W7*	I. = 16K DRAM R. = 32K or 64K DRAM
W8*	I. = Test Only R = Standard Configuration
W9*	I. = Standard Configuration R = Test Only
W10	I. = Internal Refresh R = External Refresh
W11	I. = External Refresh R = Internal Refresh
W12*	I. = 16K or 64K DRAM R = 32K DRAM

Table 1.1
Jumper Definition

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Table 1.1 (Continued)

W13*	I = 32K DRAM - Upper R = 16K or 32K Lower or 64K DRAM
W14*	I = 32K DRAM - Lower R = 16K, 32K Upper or 64K DRAM
W15	I = 18 Bit Address Bus R = 22 Bit Address Bus
W16	I = External Refresh to MEMSEL R = External Refresh isolated from MEMSEL
W17*	I = 150 ns DRAM R = 200 ns DRAM
W18*	I = 200 ns DRAM R = 150 ns DRAM
W19	I = +5v Battery Back-up R = +5v Standard
W20	I = +5v Standard R = +5v Battery Back-up

* Factory Configuration - Do not Alter!

DIP SWITCH 1

S1-1	Starting Address Select LSB
S1-2	Starting Address Select
S1-3	
S1-4	
S1-5	
S1-6	
S1-7	
S1-8	
S1-9	Starting Address Select MSB
S1-10	2K/4K I/O Space

Table 1.2
Switch Definitions



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SIZE	DWG. NO.	
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1870-1871. 1871-1872. 1872-1873.

1873-1874. 1874-1875. 1875-1876.

1876-1877. 1877-1878. 1878-1879.

1879-1880. 1880-1881. 1881-1882.

1882-1883. 1883-1884. 1884-1885.

1885-1886. 1886-1887. 1887-1888.

1888-1889. 1889-1890. 1890-1891.

1891-1892. 1892-1893. 1893-1894.

1894-1895. 1895-1896. 1896-1897.

1897-1898. 1898-1899. 1899-1900.

1900-1901. 1901-1902. 1902-1903.

1903-1904. 1904-1905. 1905-1906.

1906-1907. 1907-1908. 1908-1909.

1909-1910. 1910-1911. 1911-1912.

1912-1913. 1913-1914. 1914-1915.

1915-1916. 1916-1917. 1917-1918.

1918-1919. 1919-1920. 1920-1921.

Table 1.2 (Continued)

DIP SWITCH 2

S2-1	Memory Size LSB
S2-2	Memory Size
S2-3	Memory Size
S2-4	Memory Size MSB

1.2 UNPACKING AND INSPECTION

Follow the steps listed below to unpack and inspect the NS23M memory module:

1. Remove all packing material from shipping container.
2. Remove memory board from its container.
3. Inspect the board for damage, checking for bent parts, damaged IC's, broken wires or connectors, broken switches, etc. If any damage is found, do not attempt to install the memory.

1.3 ADDRESS RANGE SELECTION

The address range is set by assigning a bus type, selecting the proper I/O space, assigning a starting address and memory size. Refer to Table 1.3 for bus type selection, Table 1.4 and 1.5 for starting address selection, Table 1.6 for I/O space selection, and Table 1.7 for memory size selection.

Bus Type	Install/ Remove
18 Bit	Install Jumper
Address Bus	W15
22 Bit	Remove Jumper
Address Bus	W15

Table 1.3 Bus Type Selection



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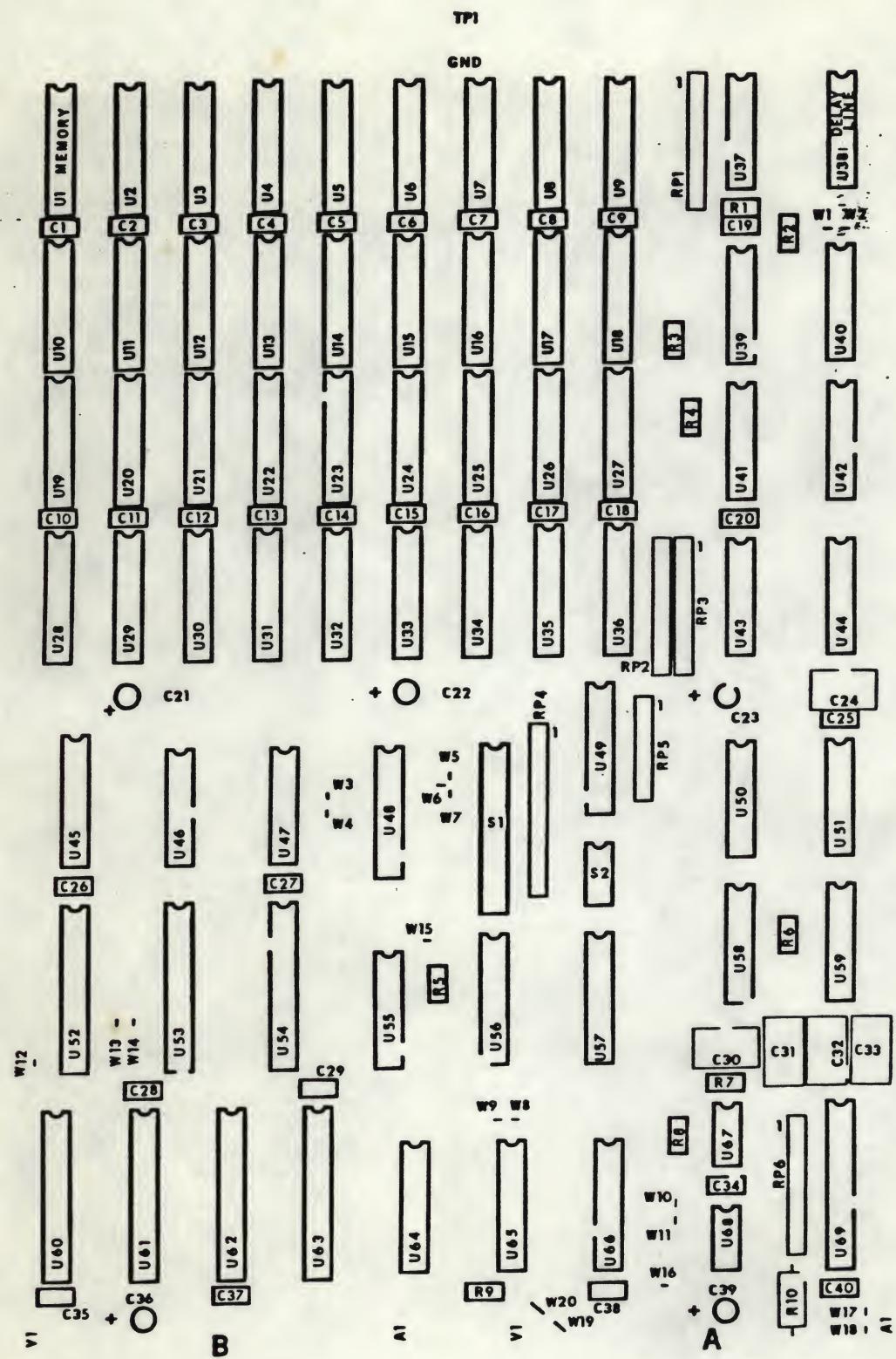


Figure 1.1 Jumper and Switch Placement



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SIZE A	DWG. NO. 409103882-001	A.
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STARTING ADDRESS*	S1-5	S1-4	S1-3	S1-2	S1-1
OK	0	0	0	0	0
4K	0	0	0	0	1
8K	0	0	0	1	0
12K	0	0	0	1	1
16K	0	0	1	0	0
20K	0	0	1	0	1
24K	0	0	1	1	0
28K	0	0	1	1	1
32K	0	1	0	0	0
36K	0	1	0	0	1
40K	0	1	0	1	0
44K	0	1	0	1	1
48K	0	1	1	0	0
52K	0	1	1	0	1
56K	0	1	1	1	0
60K	0	1	1	1	1
64K	1	0	0	0	0
68K	1	0	0	0	1
72K	1	0	0	1	0
76K	1	0	0	1	1
80K	1	0	1	0	0
84K	1	0	1	0	1
88K	1	0	1	1	0
92K	1	0	1	1	1
96K	1	1	0	0	0
100K	1	1	0	0	1
104K	1	1	0	1	0
108K	1	1	0	1	1
112K	1	1	1	0	0
116K	1	1	1	0	1
120K	1	1	1	1	0
124K	1	1	1	1	1

* In 4K word increments

** 0 = Open (OFF)
1 = CLOSED (ON)

Table 1.4 - STARTING ADDRESS SELECTION

NS	National Semiconductor Corporation		SIZE	DWG. NO.
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			SCALE	7 OF

ADDRESS RANGE	S1-9	S1-8	S1-7	S1-6
OK-128	0	0	0	0
128K-256K	0	0	0	1
256K-384K	0	0	1	0
384K-512K	0	0	1	1
512K-640K	0	1	0	0
640K-768K	0	1	0	1
768K-896K	0	1	1	0
896K-1024K	0	1	1	1
1024K-1152K	1	0	0	0
1152K-1280K	1	0	0	1
1280K-1408K	1	0	1	0
1408K-1536K	1	0	1	1
1536K-1664K	1	1	0	0
1664K-1792K	1	1	0	1
1792K-1920K	1	1	1	0
1920K-2048K	1	1	1	1

* To use addresses above 128K, 22 bit addressing must be used. In this case, the starting address will be the sum of the address in Table 1.5 and the lower limit of the range in Table 1.6.

** 0 = OPEN (OFF)
1 = CLOSED (ON)

Table 1.5. - ADDRESS RANGE SELECTION

I/O SPACE	S1-10
2K I/O	Close
4K I/O	Open

Table 1.6 I/O Space Selection



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Memory Size*	Switch Settings			
	S2-4	S2-3	S2-2	S2-1
8K	0	0	0	0
16K	0	0	0	1
24K	0	0	1	0
32K	0	0	1	1
40K	0	1	0	0
48K	0	1	0	1
56K	0	1	1	0
64K	0	1	1	1
72K	1	0	0	0
80K	1	0	0	1
88K	1	0	1	0
96K	1	0	1	1
104K	1	1	0	0
112K	1	1	0	1
120K	1	1	1	0
128K	1	1	1	1

0 = open
1 = closed

* In K words, K = 1024

Table 1.7 Memory Size

1.4 BATTERY BACK-UP

The NS23M has a separated power plane so that battery back-up may be used if desired. The module requires +5 volts only and has the battery back-up input at pin AVI. To implement battery back-up remove jumper W20 and install W19. W20 may originally be in etch which means it must be cut. The battery back-up must be able to supply 1A at +5 volts d.c. to the memory module.

1.5 INTERNAL/EXTERNAL REFRESH

Refresh may be supplied from either an internal or external source. If supplied from an external source, a refresh cycle will be initiated on a low to high voltage transition and may be either synchronous or asynchronous. To maintain valid data, 256 refresh cycles must be completed every 4 ms. This can be accomplished by initiating one cycle every 15 +/- 1us. Figure 1.2 shows the suggested external refresh timing.



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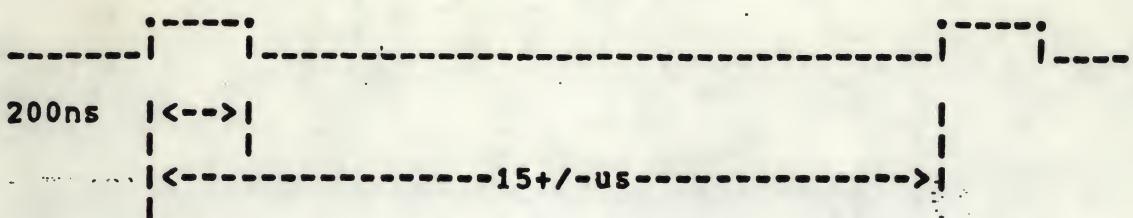


Figure 1.2 External Refresh Timing

1.6 INSTALLATION

The NS23M may be installed in any backplane wired for Q-Bus. Listed below are some guidelines:

A. Standard LSI-11 Backplanes

The NS23M Memory Card is designed to plug directly into Standard H9270 ("Quad") LSI-11 backplane/card guide assembly, and the DDV11-B ("Hex") expansion unit, the H9273-A Backplane and the H9281 backplane.

B. Precautions

In the H9270 backplane, slot one is reserved for the LSI-11 processor. The Memory Card may be inserted into any slot in this backplane with the exception of slot number one.

If the DDV11 expansion backplane is utilized, the memory card must be inserted into the A,B connectors or the C,D connectors of the backplane.

Install the card with components facing row 1, apply power and run system diagnostics. Never install or remove modules from the backplane while power is applied.

2.0 MAINTENANCE

No routine maintenance is required on the NS23M. If problems are encountered check the following:

- o Is the system configured properly? Is the bus priority daisy chain maintained?
- o Are all switches and jumpers configured properly?
- o Are the board edge contacts clean and is the board completely seated?
- o Is DC power present at the backplane?



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